**Jermaine Brown, WORK LOG**

**MILESTONE 1 WORK:**

Sunday, April 2, 2022

Met with team for [2 hours 30 min]

* We agreed on the accumulator and ran through some example code to figure out needed instructions. We decided to store data in memory and use the stack for securing data after a call to a function. 4 types of instructions identified A, AA, IA, and I.

Monday, April 3, 2022

Solo work done on assigned parts of milestone one.

Tuesday, April 4, 2022

Messaging between team on adjustments to design to account for 16 bits instead of 32 for instructions.

Wednesday, April 5, 2022

Team meeting in class [1-2] hours

* Revisions made to document to account for 16 bit instructions and established information was written down for the milestone. Code turned into instructions from rel-prime.

Revisions made later in the day after classes.

**MILESTONE 2 WORK:**

N/A

**MILESTONE 3 WORK:**

Sunday, April 24, 2022

Team meeting

* Discussed and created final Datapath. Decided to go with rising edge clock for now and not falling edge.
* Work distributed to team members, given integration plan and testing.

Tuesday, April 26, 2022

Solo work decided to go with 4 subsystems, then 2 more made up of groups of 2 subsystems for work moving forward

Wednesday, April 27, 2022

In class work

* Decided to go with 4 subsystems before creating whole Datapath and not two more.

Solo work

* Finished writing tests for subsystems.

**MILESTONE 4 WORK:**

Saturday, April 30, 2022

Team meeting

* Divided work and set deadlines as specified at the top of our document.

Sunday, May 1, 2022

Solo Work

* Implemented 2-bit mux but no testing. File completed but not committed.

Monday, May 2, 2022

Solo Work

* Made tests for 2-bit mux and began making tests for Alu component.

Tuesday, May 3, 2022

Class and Solo Work

* Finalized tests for Alu and 2-bit mux component
* Partial design for ALU subsystem but needs 3-bit mux for completion.
* Work committed and pushed.

**MILESTONE 5 WORK:**

Sunday, May 8, 2022

Team meeting

* Divided work Zeen and Athena for control and Helen and I finishing the Verilog implementation.

Tuesday, May 10, 2022

Solo Work

* Began working in top level Verilog but only ALU and PC subsystems are done.

Wednesday, May 11, 2022

Solo Work

* Added wires to top level accumulator still missing memory
* Discussed how to approach tests

**MILESTONE 6 WORK:**

Sunday, May 15, 2022

Team meeting

* Met and discussed testing assignments. While waiting on memory and control from Zeen I promised to work on testing components and adjusting design document.

Monday, May 16, 2022

Solo Work

* Checked documentation for mistakes in syntax and not clear details.

Tuesday, May 17, 2022

Missed class, no work done.

Wednesday, May 18, 2022

Solo Work

* Removed Clock from ALU and tested.
* Removed many syntax errors from PC with shift\_left on ZE
* Removed Syntax errors on accumulatorFull and added output from Memory subsystem to Wire subsystem for I